APPLICATION UNDER UNITED STATES PATENT LAWS

Invention: **DIGITAL ADAPTIVE EQUALIZER FOR T1/E1 LONG HAUL TRANSCEIVER**

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This is a:

[ ] Provisional Application

[X] Regular Utility Application

[ ] Continuing Application

[ ] PCT National Phase Application

[ ] Design Application

[ ] Reissue Application

[ ] Plant Application

SPECIFICATION

DIGITAL ADAPTIVE EQUALIZER FOR T1/E1 LONG HAUL TRANSCEIVER

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to T1/E1 type communications. More particularly, it relates to the implementation of a digital adaptive equalizer for a T1 or E1 long haul transceiver.

2. Background of Related Art

Telecommunications and more recently data communications commonly utilize T1 or E1 rate long haul transceivers for transmitting large amounts of data. A T1 type signal (1.544 Mb/s) is a standard 24 channel digital communication standard commonly used in North America. An E1 type signal (2.048 Mb/s) is a standard 30 voice channel or 32 payload channel digital communication standard commonly used in Europe. However, because of the similarities in the data structure and physical layer characteristics of T1 and E1 lines, many commercial components are capable of supporting either a T1 or an E1 standard, often with a bit setting or swap of a termination impedance.

As is known, data transmissions suffer dispersion and other debilitating degradations during transmission, particularly when transmitted over a twisted pair and/or cable.

In particular, Fig. 9 depicts the affects of a transmission path **910** between a T1/E1 transmitter **902** and a complementary T1/E1 receiver **904**. The transmission path **910** (e.g., twisted pair, coaxial cable, etc.) typically causes dispersion, attenuation, and/or other distortion with respect to a frequency domain as depicted in Fig. 9, which is ideally compensated by an analog equalizer **912** in the T1/E1 receiver **904**.

Conventional T1 or E1 equalizers **912** are analog devices included in the T1/E1 receiver **904** which are specifically adapted and designed to cancel the affects of the known transmission path **910** (e.g., twisted pair, coaxial cable, etc.) and a known length of that transmission path **910**, by equalizing the received signal before processing. Thus, a conventional analog equalizer is chosen or designed based on the specific type of cable used, and on the specific length of the cable. Even given a same type cable, generally speaking the longer the cable, the more affected the received T1/E1 signal is by transmission through the path **910**.

Conventional analog devices are typically designed with the specific cable type and sometimes even the length of the cable in mind. Thus, as cable length changes and/or as cable types change, conventional analog T1/E1 equalizers require physical changes to the circuit board containing the T1/E1 long haul transceiver to allow proper equalization of the received T1 or E1 signal. This poses delays and reliability issues when changes to a system are incurred, e.g., when increasing or decreasing the length of a T1/E1 cable.

There is a need for a more flexible T1/E1 equalizer which adapts to changes in T1/E1 cable type and/or length without requiring physical hardware changes to the receiving T1/E1 long haul device.

SUMMARY OF THE INVENTION

In accordance with the principles of the present invention, a digital adaptive equalizer for a data communication path comprises a first programmable filter capable of being programmed to implement any of a plurality of filter transfer functions. A filter selector selects any one of the plurality of filter transfer functions for the first programmable filter. A second digital filter receives an output from the first programmable filter.

A method of digitally equalizing a received T1/E1 data signal in accordance with another aspect of the present invention comprises firstly filtering the received T1/E1 data signal using a first digital filter. An output of the first digital filter is adaptively adjusted to accurately match an inverse response of a transmission channel used to transmit the received T1/E1 data signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Features and advantages of the present invention will become apparent to those skilled in the art from the following description with reference to the drawings, in which:

Fig. 1 shows an exemplary embodiment of a front end of a T1/E1 receiver including a digital adaptive equalizer comprising three main blocks, in accordance with the principles of the present invention.

Fig. 2 shows a block diagram of a digital adaptive equalizer including two filters and a control block, in accordance with the principles of the present invention.

Fig. 3 is a detailed block diagram of the IIR filter shown in Fig. 2.

Fig. 4 shows a schematic of a particular implementation of the IIR filter shown in Figs. 2 and 3.

Fig. 5 is a detailed block diagram of the filter selector shown in Fig. 2.

Fig. 6 is a more detailed block diagram of the filter selector shown in Figs. 2 and 5.

Fig. 7 shows a block diagram of the adaptive FIR filter shown in Fig. 2.

Fig. 8 shows a more detailed block diagram of an exemplary implementation of the adaptive FIR filter shown in Figs. 2 and 7.

Fig. 9 depicts the affects of a transmission path between a T1/E1 transmitter and a complementary T1/E1 receiver having a conventional equalizer.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The present invention relates to the implementation of a digital adaptive equalizer for a T1/E1 long haul transceiver (i.e., the receiver portion) which is capable of adapting to a wide range of cable types, cable lengths, and/or other data transmission impairments. The digital adaptive equalizer corrects for or equalizes impairments caused in a T1 or E1 type signal which has presumably been degraded upon transmission, particularly where the cable type and/or length may be unknown (or have changed). The digital adaptive equalizer for T1/E1 long haul transceivers in accordance with the principles of the present invention can be implemented easily using low voltage digital technology. The invention has particular application when the T1/E1 signal has been received through an unknown channel (e.g., an unknown cable type, length, and/or other impediments to ideal transmission).

The digital adaptive equalizer contains two filter blocks, i.e., an IIR filter and a FIR filter, together with a filter selector block.

The IIR filter receives the digitized samples of a received analog signal (e.g., from a suitable analog-to-digital (A/D) converter). Preferably, the IIR includes a programmable set of coefficients, wherein each programmable set of coefficients represents a different IIR filter. Preferably, each set of coefficients is chosen to best represent the expected (or anticipated) cable types and/or lengths for which the T1/E1 long haul transceiver is specified. Only a few sets of coefficients are found to be necessary to allow proper digital equalization of a large number of cable types and/or lengths.

The particular set of coefficients to be programmed (and thus the particular IIR filter) is chosen, e.g., using an error estimation algorithm. The error estimation algorithm detects which IIR filter would be optimum for use given a current set of conditions. The error estimation algorithm may be operated as often as necessary, e.g., at start up of a communication system. Thus, whenever a cable type and/or length might be changed (e.g., whenever the system is moved or a cable is replaced), instead of requiring a physical change of analog components as in conventional analog equalizers, a digital adaptive equalizer for T1/E1 long haul applications need only be re-booted.

A filter selector block selects a desired set of coefficients corresponding to the best IIR filter. The coefficients may be programmed into volatile memory (e.g., RAM) or non-volatile memory (e.g., Flash). Alternatively, the coefficients may be hardwired into the IIR filter.

The back end of the digital adaptive equalizer contains an adaptive finite impulse response (FIR) filter. In the disclosed embodiment, the FIR filter uses a least mean square (LMS) algorithm for adaptation to the unknown or changed T1 or E1 transmission channel or medium. The adaptive FIR filter adjusts the output from the IIR filter to accurately match the inverse response of the unknown channel used to transmit the received T1/E1 signal.

Preferably, the adaptive LMS FIR filter is modified to work under the main problems a T1/E1 signal presents for digital adaptive algorithms, i.e., the fact that the source is correlated and the periodic patterns that the signal might contain.

A restored T1 or E1 signal is output from the FIR filter, and thus from the digital adaptive equalizer, in accordance with the principles of the present invention.

Fig. 1 shows an exemplary embodiment of a front end **171** of a T1/E1 receiver including a digital adaptive equalizer comprising three main blocks, in accordance with the principles of the present invention.

In particular, in Fig. 1, the front end **171** receives a raw T1 or E1 data signal from a transmission path (wired or wireless). The front end **171** includes an analog portion **171a** and a digital portion **171b**.

An automated gain control (AGC) in the analog portion **171a** of the front end **171** receives the raw data signal in analog form, and appropriately couples the received signal to an analog-to-digital (A/D) converter **110** (e.g., an 8-bit A/D converter in the disclosed embodiment). In the disclosed embodiment, the PGA **112** maximizes the dynamic range of the received raw data signal to provide the A/D converter **110** with a constant envelope (e.g., +1 to –1).

The principles of the present invention relate equally to data transmission techniques and data rates other than those specifically at T1 or E1 rates. In the example of the disclosed embodiment using T1 and E1 data rates, the A/D converter **110** is an 8-bit converter which is sampled at a rate of four samples per symbol (i.e., 4 x f). In the case of a T1 (i.e., 1.544 Mb/s) digital adaptive equalizer, the input data signal is sampled at four times the T1 rate, or 6.176 MHz. Similarly, in the case of an E1 (i.e., 2.048 Mb/s) digital adaptive equalizer, the input data signal is sampled at four times the E1 rate, or 8.192 MHz.

In the digital portion 171b of the front end 171, the equalizer 100 receives the 8-bit samples from the A/D converter 110, equalizes the digitized input data signal, and outputs 8-bit samples. Of course, the present invention relates equally to sample sizes other than those of the disclosed exemplary embodiment, e.g., 10 bits, 12 bits, 16 bits, etc.

An interpolator **102** in the digital portion **171b** of the front end **171** interpolates the signals from the equalizer **100** into an interpolated output signal having a much faster output sampling rate. For

example, the exemplary interpolator **102** interpolates and outputs samples at 96 times the T1 or E1 rate (i.e., 148.224 MHz or 196.608 MHz, respectively). The output of the interpolator **102** is passed to a timing recovery stage to achieve the requirements (e.g., telecommunications standards such as jitter specifications) of a recovered T1/E1 signal.

Fig. 2 shows a block diagram of a digital adaptive equalizer **100** including two filters and a control block, in accordance with the principles of the present invention.

In particular, the digital adaptive equalizer **100** includes an infinite impulse response (IIR) filter **202**, followed by a filter selector **204**, and then by a finite impulse response (FIR) filter **206**.

The IIR filter **202** in the disclosed embodiment is a 7^{th} order filter. The IIR filter **202** effectively opens the signal eye-diagram of the received digitized data signal.

The filter selector **204** selects the optimum IIR filter, and programs the related coefficients into the IIR filter **202** based on that selection. The filter selector **204** also performs timing and process control for the equalizer **100**, and converts the 9-bit output from the IIR filter **202** into 8-bit samples for use by the FIR filter **206**.

The adaptive FIR filter **206** includes a finite impulse response filter having, e.g., 16 taps. In the disclosed embodiment, the adaptive FIR filter **206** utilizes a least mean squares (LMS) fit, and completes the equalization of the input data samples.

In a specific application, four separate sets of coefficients are available for use by the IIR filter **202**, effectively transforming the IIR filter **202** into any one of four different IIR filters without requiring a physical hardware change. The four sets of coefficients are established to represent the IIR filters **202** that best fit to the overall conditions of a wide set of cable types and/or lengths.

The filter selector **204** tests each of the possible IIR filters, and selects at that time the particular IIR filter which yields the least error in the filter selector **204**. The output of the selected IIR filter **202** is passed to the adaptive FIR filter **206**, which improves the total equalization of the received data signal.

Fig. 3 is a detailed block diagram of the IIR filter **202** shown in Fig. 2.

In particular, in Fig. 3, the IIR filter **202** comprises an IIR filter core **302**, and a coefficient register area **304** storing the various sets (e.g., 4 sets) of coefficients for the IIR filter core **302**. The coefficient registers **304** are selected by the filter selector **204**, and the selected coefficient set is loaded into the IIR core **302**. In the disclosed embodiment, only one set of coefficients are loaded into the IIR filter core **302** at any one time, as selected by the 2 bit wide selector bus SDOUT from the filter selector **204**.

Preferably, the available sets of coefficients for the IIR filter **202** are loaded into the coefficients register area **304** prior to startup of the equalization process.

In the disclosed embodiment, the IIR filter **202** implements the following equations:

$$y[n] = a_1 x[n] + a_2 x[n-1] + \ldots + a_8 x[n-7] - b_2 y[n-1] - \ldots - b_7 y[n-7]$$

$$H(z) = \frac{a_1 + a_2 z^{-1} + a_3 z^{-2} + a_4 z^{-3} + a_5 z^{-4} + a_6 z^{-5} + a_7 z^{-6} + a_8 z^{-7}}{1 + b_2 z^{-1} + b_3 z^{-2} + b_4 z^{-3} + b_5 z^{-4} + b_6 z^{-5} + b_7 z^{-6} + b_8 z^{-7}}$$

Fig. 4 shows a schematic of a particular implementation of the IIR filter **202** shown in Figs. 2 and 3.

In particular, in Fig. 4, the IIR filter **202** includes a plurality of 8-bit coefficients **412-420**, **440-446** which are loaded with a selected set of

coefficients from the coefficients register **304**, based on an IIR filter selection from the filter selector **204** over the SDOUT bus.

Input samples are loaded into 8-bit registers **402-410** constituting an input delay line. The input samples are shifted through the 8-bit registers **402-410** every 1/4T.

Output samples are loaded into output 9-bit registers **448-454** constituting an output feedback delay line.

Multiplication operations are performed in the various multipliers **422-438**, and the results are appropriately summed in summer **460**, to ultimately arrive at the desired equations for the IIR filter **202**.

Fig. 5 is a detailed block diagram of the filter selector **204** shown in Fig. 2.

In particular, as shown in Fig. 5, the filter selector comprises a programmable gain amplifier **502**, an error estimator **506**, a peak detector **504**, and a state machine and control block **508**.

The PGA **502** converts the 9-bit input signal from the IIR filter **202** into an 8-bit output signal, the error estimator **506** calculates the total absolute error of the current IIR filter, and the peak detector **504** detects the maximum value of the input IIR filtered data signal.

Fig. 6 is a more detailed block diagram of the filter selector **204** shown in Figs. 2 and 5.

In particular, the PGA **502** includes a multiplexer **612** which selects eight bits from the 9-bit input IIR filtered data samples, depending upon on the value of the maximum data sample detected by the peak detector **504**. The PGA **502** includes a divide by 2 block **608**, and a least significant bit block, each fed into and selected by the multiplexer **612**.

The peak detector **504** stores the value of the maximum data sample detected in the 9-bit register **604**. The peak detector **504** includes a comparator **602** to compare an input 9-bit data sample to a currently established maximum data value maintained in a 9-bit register

604. The most significant 8 bits of the maximum value are selected in block **606**, which is divided by 2 in divider **630**.

The error estimator **506** includes a slicer **614**, a summer **616**, an absolute value determiner **618**, another summer **620**, a 24-bit register **624**, a comparator **626**, and another 24-bit register **628**.

The error estimator **506** calculates the total absolute error by comparing the input IIR filtered data sample to a sliced version of the same signal as follows.

$$TAE = \sum_{1}^{16384} |x[n] - a[n]|$$

where *x[n]* is the input signal, and *a[n]* is the sliced signal.

The slicer **614** in the error estimator **204** creates the sliced signal from the maximum value detected. The threshold of the slicer **614** is equal to the maximum value divided by two (i.e., T=M/2).

$$if\_x[n] \rangle T, a[n] = M$$

$$if\_-T \langle x[n] \langle T, a[n] = 0$$

$$if\_x[n] \langle -T, a[n] = -M$$

The error estimator **506** stores the total absolute error detected using each of the available IIR filters (e.g., each of the 4 IIR filters in the given example). After each of the available IIR filters are tested, the error estimator **506** and the control block **508** outputs the selection of the IIR filter providing the least absolute error.

In operation, the filter selector **204** waits 256 samples for the IIR filter transient to be completed. The next 16128 data samples are used by the peak detector **504** to find the maximum value of the input IIR

filtered data, and the last 16384 data samples are used by the error estimator **506** to calculate the total absolute error.

Fig. 7 shows a block diagram of the adaptive FIR filter **206** shown in Fig. 2, and Fig. 8 shows a more detailed block diagram of an exemplary implementation of the adaptive FIR filter **206** shown in Figs. 2 and 7.

In particular, as shown in Figs. 7 and 8, the adaptive FIR filter **206** is implemented with 16 taps. As shown in Fig. 7, the input samples are stored in a delay chain of 8-bit registers **702-710** (**802-808** in Fig. 8), and shifted every 1/4T. Coefficients for the FIR filter **206** are stored in 16-bit registers **712-716** (**816** in Fig. 8).

In the implementation of Figs. 7 and 8, only the eight most significant bits out of the 16 bits of the filter coefficients are used to evaluate the output. The remaining eight bits are used to store the small corrections to the coefficients **712-716**, and thus adaptively adjusts the FIR filter **206**.

The FIR filter **206** preferably includes an adaptive algorithm, e.g., a least mean squares algorithm. A least mean squares algorithm was chosen in the given example because of the properties of a T1/E1 signal, e.g., correlated source, periodic patterns, etc. The FIR filter **206** outputs 8-bit samples, and implements the following equations.

FIR equation:

$$y[n] = c_1 x[n] + c_2 x[n-1] + \ldots + c_{15} x[n-14] + c_{16} x[n-15]$$

Coefficients correction (LMS algorithm):

$$C_i(new) = C_i(old) - k \cdot x[n-i] \cdot \left(y[n] - r[n]\right)$$

where *r[n]* is the reference signal used to measure the error of the output signal, and *k* is the step size.

The signal output from the adaptive FIR filter **206** is sliced using a slicer **822** as shown in Fig. 8 to generate the reference signal *r[n]*. In particular, the slicer **822** implements the following equations:

$$if\_y[n] \rangle 0.5, r[n] = 1$$

$$if\_y[n] \langle -0.5, r[n] = -1$$

$$otherwise, r[n] = 0$$

The coefficients (**712-716** in Fig. 7, **816** in Fig. 8) are updated every sample.

The step size in the adaptive FIR filter **206** is a number always lower than one, e.g.,1/2, 1/4, 1/16, etc. The step size is reduced as the algorithm converges, and can be set equal to zero (i.e., no coefficients correction).

In order to accomplish fast convergence of the least mean square algorithm, the initial value of the coefficients is set to the autocorrelation function of an AMI-RZ (amplitude mark inversion, return to zero) signal, characteristic in the transmission of a T1/E1 signal. It is common to transmit periodic signals in a T1/E1 transmission. Some alarms to be transmitted have this characteristic. A periodic pattern causes a major problem to equalization algorithms.

This issue is solved, e.g., by using a periodic pattern detector **113** as shown in Fig. 1. When a periodic pattern is detected by

the periodic pattern detector **113**, the adaptive equalization is frozen and the output samples come directly from the periodic pattern detector **113**.

A digital, adaptive equalizer in accordance with the principles of the present invention provides adaptation to a much larger range of cable types and/or lengths, particularly with automatic reprogramming of coefficients for the IIR filter.

While the invention has been described with reference to the exemplary embodiments thereof, those skilled in the art will be able to make various modifications to the described embodiments of the invention without departing from the true spirit and scope of the invention.